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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,932	04/12/2004	Masao Murade	119271	2127

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EXAMINER	
MA, CALVIN	

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/821,932	MURADE, MASAO	
	Examiner	Art Unit	
	CALVIN C. MA	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☒ Claim(s) *13 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed on 2/10/2009 has been entered and considered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-7, 9 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurashina (US Patent: 6,597,413) in view of Hirabayashi (US Patent: 6,577,371) further in view of Shimomaki (6,678,017) and further in view of Morishita (US Patent: 6,777,973).

As to claim 1, Kurashina discloses an electro-optical device (see Fig. 1) comprising:

a substrate (i.e. TFT array substrate 10) (see Fig. 3, Col. 15, Line 8); data lines (6a) formed above the substrate (10) and extending in a predetermined direction (i.e. the data line are arrangement orthogonally and there for has a predetermined vertically aligned direction) (see Fig. 6) and scanning lines (3a)formed above the substrate (10) and extending in a direction (i.e. being perpendicular to the data line) (see Fig. 6)

intersecting the data lines (i.e. the data lines 6a and scanning lines 3a are clearly intersecting and above the substrate 10) (see Fig. 6, Fig. 7, Col. 19, Lines 63-67, Col. 20, Lines 1-23);

switching elements (i.e. switching TFT 30) to which scanning signals (G1 ,G2,..Gn) are supplied from the scanning lines (3a) (see Fig. 6-10, Col. 19, Lines 25-36);

pixel electrodes (9a) to which image signals(S1, $2, .. Sn) are supplied from the data lines (6a) via the switching elements (30) (i.e. the TFT clearly is connected to the data line and the pixel electrode) (see Fig. 7, Col. 19, Lines 16- 29);

a relay electrode that electrically connects one of the switching elements to one of the pixel electrode (i.e. since the switching is a transistor it has an relay electrode that electrically connect the transistor to the pixel electrode 9a to the semiconductor layer 1a forming the TFT switch) (see Fig. 3, Col. 13, Lines 15-30);

an image display region (i.e. the actual displaying area of the display with respect to the substrate) defined as a region of the substrate (10) in which the pixel electrodes (9a) and the switching elements (30) are formed (i.e. the image display area is where the TFT 30 and the pixel electrode 9a reside) (see Fig. 7, Col. 19, Lines 50-53);

a peripheral region (i.e. area surrounding the display area) defining the periphery of the image display region (area of 9a and 30) (see Fig 7, Col. 19, Lines 50-53).

storage capacitors (70) provided above the image display region to retain potentials of the pixel electrodes (9a) for a predetermined period of time (i.e. since the

storage capacitor 70 overlaps the pixel electrode 9a it is in the image display region) (see Fig. 7, Col. 20, Lines 1-23); and

a capacitor wire (i.e. capacitive line,11a) which supplies a predetermined potential to capacitor electrodes forming the storage capacitors (70) (see Fig. 7, Col. 19, Lines 50-63) and which is formed as the same film as that for electrodes forming the exterior circuit connection terminals (i.e. since the entire transistor for the TFT LCD system is called a thin-film transistor the capacitor electrode and the external circuit connection must be formed on the same thin-film material for the over display) (see Fig. 1, Col. 1, Lines 37-40).

Kurashina does not explicitly teach a driver disposed in the peripheral region; exterior circuit connection terminals comprising electrodes provided in the peripheral region at a position between the driver and a peripheral edge of the substrate. Hirabayashi teaches a driver (i.e. 21 data lines driver) disposed in the peripheral region (i.e. the data line driver is situated on the substrate and is in the peripheral region surrounding the display area) (see Fig. 1, Col. 12, Lines 1-39);

exterior circuit connection terminals (i.e. 26 data pads that will allow data to be inputted from outside the circuit) provided in the peripheral region at a position between the driver (21) and a peripheral edge (i.e. the edge of the LCD substrate) of the substrate (i.e. clearly the data pad 26 are situated between the data driver 21 and the edge of the substrate) (see Fig. 1, Col. 12, Lines 1-39).

Hirabayashi also teaches and a capacitor wire (i.e. capacitive line,1 la) which supplies a predetermined potential to the capacitor electrodes comprising capacitor

electrodes (i.e. 7a, 10 wire of the C retention capacitor) and which is formed as the same film as that for electrodes forming the exterior circuit connection terminals (i.e. the data pad electrode 26a) (see Fig. 22, Col. 3, Line 62- Col. 4, Line 19).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have added the external data driver, and the same layer data pad capacitor electrode design to the overall substrate design of Kurashina in order to improve the interlayer insulation (see Hirabayashi, Col. 6, Lines 1-11).

Also Kurashina does not explicitly teach a capacitor wire which is formed of a same material as that for electrodes forming the exterior circuit connection terminals. Shimomaki teaches teach a capacitor wire which is formed of a same material as that for electrodes forming the exterior circuit connection terminals (i.e. scan line 9, a lower metal layer 17a for a connecting pad 17, and auxiliary capacitor line 11 are also formed from Aluminum based metal film, in this way both the capacitor wire 11 and external connection pad are formed by the aluminum based material) (see Shimomaki, Fig. 1,2, Col. 8, Lines 1-21).

Therefore, it would have been obvious for one of ordinary skill in the art at the time the invention was made to have used the aluminum material design of Shimomaki for the display circuitry design of Kurashina in order to create a circuitry design that reduce the resistance and decrease the width of the data lines. (see Shimomaki, Col 4, Line 33-38)

However Kurashina, Hirabayashi, and Shimomaki does not teach the relay electrode are of the same material as the capacitor wire, and the external connection

terminals, Shimomaki teach the relay electrode (i.e. the source electrode S) being formed with chromium material instead of aluminum based one (see Shimomaki, Fig. 5, Col. 8, Lines 50-60). Morishita teaches the relay electrode is formed by either aluminum or chromium material (see Morishita, Col. 6, Lines 50-58).

Therefore it would have been obvious for one of ordinary skill in the art at the time the invention was made to have used the aluminum structure for relay electrode used in Morishita in the overall manufacturing layer process of Shimomaki in order to made it easier to detect fault in the display device (see Morishita, Col. 2, Lines 43-47).

As to claim 2, Kurashina teaches the electro-optical device according to claim 1, the capacitor wire (1 la) formed on the data lines (6a) with a first interlayer insulating film (12) interposed therebetween (see Fig. 7, Col. 19, Lines 50-63).

As to claim 3, Kurashina teaches the electro-optical device according to claim 1, the capacitor wire (1 la) formed in a layer located immediately under a layer including the pixel electrodes (9a) (i.e. the capacitor wire 11 is clearly formed under the pixel electrode 9a) (see Fig. 7, Col. 19, Lines 50-63).

As to claim 4, Kurashina teaches the electro-optical device according to claim 1, the capacitor electrodes (70-3) provided below the data lines (6a) with a second interlayer insulating film (312) interposed there between (i.e. the capacitor electrode (i.e.

part of the capacitor 70-3 is clearly formed under the pixel electrode 6a with insulating film 311 in between) (see Fig. 7, Col. 19, Lines 63-67, Col. 20, Lines 1-23).

As to claim 5, Kurashina teaches the electro-optical device according to claim 1, further comprising: a scanning line drive circuit (104), a potential supplied to the capacitor wire (1 la) including a potential supplied to the scanning line drive circuit (i.e. it is inherent that since the scanning line is directly connected to the capacitor wire 1 la that the potential supplied are from the scanning line drive circuit (104) (see Fig. 7, Fig. 42, Col. 37, Lines 41-55).

As to claim 6, Kurashina teaches the electro-optical device according to claim 1, further comprising: a counter substrate (20) and a counter electrode (21) provided above the counter substrate (20) (see Fig. 3, Col. 15, Lines 21-25);
a potential supplied to the capacitor wire including a potential supplied to the counter electrode (it is inherent that in order to form a working LCD cell shown in Fig. 42, the two electrodes that exist on the two substrates forming the ,. cell uses the same power inputted from the external electrode (102) as the capacitor line 1 la in Fig. 7, which describe one possible lay out of the LCD cell design) (see Fig. 7, Fig. 41, Fig. 42, Col. 15, Lines 6-26, Col.37, Lines 41-67).

As to claim 7, Kurashina teaches the electro-optical device according to claim 1, the capacitor wire including a shading material (1 la light shielding film) (i.e. the first light

shielding film 1 la also serving as capacitive line) (see Fig. 7, Col. 19, Lines 50-53).

As to claim 9, Kurashina teaches the electro-optical device according to claim 1, the capacitor wire having a lattice pattern in the image display region when viewed in plan (i.e. the capacitor wire 1 la in the clearly has a regular repeating grid pattern that resemble a lattice) (see Fig. 23, Col. 28, Lines 23-36).

Claim 12 is rejected on the same ground as claim 1, since the same limitation is cited.

4. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kurashina in view of Hirabayashi, further in view of Shimomaki and further in view of Morishita as applied to claim 1 above, and further in view of Kim (U.S.P.G. Pub 200610102903).

As to claim 8, Kurashina and Hirabayashi teach the electro-optical device according to claim 1 but does not explicitly teach the capacitor wire having a multilayer structure including different materials. Kim teaches the capacitor wire (25) having a multilayer structure including different materials (i.e. the storage electrode line 25 have double-layer or triple layer structure for instance Cr/AI or AI alloy, or AI alloy/Mo may be used) (see Fig. 19, Col. 12, Line 16 - Col. 13, Line 6)

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the capacitor lines of Kurashina with Kim's

design with multiple layers with different materials in order to prevent non- uniformity in the display due to difference in parasitic capacitance (see Kim, Col. 1, Lines 50-67).

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kurashina in view of Hirabayashi, further in view of Shimomaki and further in view of Morishita as applied to claim 1 above as applied in claim 9, and further in view of Matsushima et al. (U.S.P.G. Pub 2003/0202800).

As to claim 10, Kurashina and Hirabayashi teaches the electro-optical device according to claim 9, the capacitor wire formed in the lattice pattern, but does not teach having intersections each having at least one of approximately triangle shaped section at least one of four corners of the intersections. Matsushima teaches having intersections each having at least one of approximately triangle shaped section (112) (i.e. triangular conductor) at least one of four corners of the intersections. (i.e. by providing a triangular conductor on the inner angular portion thereof and further restrains capacitance from fluctuating between the inner angular portion of the signal wiring conductor) (see Fig. 3, [0052])

Therefore it would be obvious for one skill in the art at the time of the invention to have modified the capacitor wire of Kurashina with the angular design of Matsushima in order to restrain capacitance from fluctuation (see [0052], Matsushima).

6. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kurashina in view of Hirabayashi, further in view of Shimomaki and further in view of

Morishita as applied to claim 1 above, and further in view of Murade (US Patent 6,480,244).

As to claim 11, Kurashina and Hirabayashi teaches the electro-optical device according to claim 1, but does not teach a step-adjusting film under a region corresponding to the exterior circuit connection terminals, the step- adjusting film adjusting the height of the capacitor wire and that of the exterior circuit connection terminals to be approximately equivalent to each other with respect to the surface of the substrate.

Murade, teaches step-adjusting film under a region corresponding to the exterior circuit connection terminals, the step-adjusting film adjusting the height of the capacitor wire and that of the exterior circuit connection terminals to be approximately equivalent to each other with respect to the surface of the substrate (i.e. adjusting the film thickness of the lift-up film to be approximately equal to that of the exterior circuit connection terminals (scanning line) and capacitor line) (see Col. 3, Lines 51-58). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have provided the step adjustment capability of Murade's design to the display control circuit layout of Kurashina and Hirabayashi to avoid decreasing in process yield, when pixels are made fine (see Murade, Col. 2, Lines 43-52).

Allowable Subject Matter

Claims 13 and 14 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of

the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments filed 1/23/2009 have been fully considered but they are not persuasive.

The applicant in page 5-7 of the reply argues with respect to the claims 1-7, 9 and 12 that the prior arts Kurashina, Hirabayashi, Shimomaki, Morishita does not teach having a the electrode, capacitor wire being formed with the same material and in the same film. The examiner disagrees because the prior art Morishita teaches that the material of the TFT structure being of the several commonly used metals having good conductive properties this disclosure is merely cited to show that the design of the layered structure is well known by one skilled in that art to have a necessary conductive layer structure to allow for electrons to be carried to the components formed on the TFT film. Therefore in the broad sense the TFT display structure is a film that are formed with conductive metallic material as taught by Morishita when in view of the TFT display film structure of Hirabayashi, Shimomaki, Morishita.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CALVIN C. MA whose telephone number is (571)270-1713. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on 571-272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Calvin Ma

May 9, 2009

/Chanh Nguyen/
Supervisory Patent Examiner, Art Unit 2629